

WHAT IS CLAIMED IS:

1. A semiconductor component, comprising:
a substrate having a major surface;
a trench having first and second sidewalls extending from the major surface into the substrate;
a first column of memory cells adjacent the first sidewall; and
a trench line disposed in the trench, wherein the trench line is electrically coupled to the first column of memory cells.
2. The semiconductor component of claim 1, wherein the first column of memory cells comprises at least one memory cell having a gate structure, a drain region, and a source region.
3. The semiconductor component of claim 2, further including a first connector, wherein the first connector electrically couples one of the source region or the drain region to the trench line.
4. The semiconductor component of claim 3, further including a second connector, wherein the second connector electrically couples the other of the source region or the drain region to the trench line.
5. The semiconductor component of claim 3, wherein the trench line serves as a bit line.
6. The semiconductor component of claim 2, further including a drain connector, wherein the drain connector electrically couples the drain region of the at least one memory cell to the trench line.
7. The semiconductor component of claim 6, further including a source connector, wherein the source connector electrically couples the source region of the at least one memory cell to the trench line.

8. The semiconductor component of claim 2, further including a source connector, wherein the source connector electrically couples the source region of the at least one memory cell to the trench line.
9. The semiconductor component of claim 8, further including a second column of memory cells, wherein the second column of memory cells is adjacent the second sidewall and comprises at least one memory cell having a gate structure, a drain region, and a source region.
10. The semiconductor component of claim 8, further including another drain connector, wherein the another drain connector electrically couples the drain region of the at least one memory cell of the second column of memory cells to the trench line.
11. The semiconductor component of claim 8, further including another source connector, wherein the another source connector electrically couples the drain region of the at least one memory cell of the second column of memory cells to the trench line.
12. The semiconductor component of claim 1, further including a second column of memory cells, wherein the second column of memory cells is adjacent the second sidewall and comprises at least one memory cell having a gate structure, a drain region, and a source region.
13. A memory device, comprising:
 - a first memory cell having a gate structure, a drain region, and a source region;
 - a second memory cell having a gate structure, a drain region, and a source region,wherein the source region of the second memory cell is coupled to the source region of the first memory cell, and wherein the first and second memory cells cooperate to form a first column of memory cells; and
 - a first trench line adjacent the first column of memory cells, wherein the source regions of the first and second memory cells are coupled to the first trench line.
14. The memory device of claim 13, further including a second trench line adjacent the first column of memory cells, wherein the drain regions of the first and second memory cells are coupled to the second trench line.

15. The memory device of claim 14, further including:
a third memory cell having a gate structure, a drain region, and a source region; and
a fourth memory cell having a gate structure, a drain region, and a source region,
wherein the source region of the fourth memory cell is coupled to the source region of the
third memory cell and the source regions of the third and fourth memory cells are coupled
to the second trench line, and wherein the third and fourth memory cells cooperate to form
a second column of memory cells.
16. The memory device of claim 15, wherein the second trench line is between the first
and second columns of memory cells.
17. The memory device of claim 15, further including a third trench line adjacent the
second column of memory cells.
18. The memory device of claim 17, wherein the drain regions of the third and fourth
memory cells are coupled to the third trench line.
19. The memory device of claim 18, wherein the first trench line serves as a first bit
line, the second trench line serves as a second bit line, and the third trench line serves as a
third bit line.
20. The memory device of claim 15, further including a first bit line coupled to the
drain regions of the first and second memory cells.
21. The memory device of claim 20, further including a second bit line coupled to the
drain regions of the second and third memory cells.
22. The memory device of claim 13, further including a first bit line coupled to the
drain regions of the first and second memory cells.
23. A method for manufacturing a semiconductor component, comprising:
providing a semiconductor substrate having a major surface;

forming a first trench in the semiconductor substrate, the first trench extending from the major surface into the semiconductor substrate and having first and second sidewalls and a floor;

forming a trench line in the trench;

forming first and second semiconductor inserts between the trench line and the respective first and second sidewalls of the trench;

forming a first doped region in a portion of the semiconductor substrate adjacent the first sidewall of the first trench;

forming a second doped region in another portion of the semiconductor substrate adjacent the first sidewall of the first trench; and

forming a first connector, wherein the first connector electrically couples the first doped region to the second doped region.

24. The method of claim 23, wherein forming the trench line comprises:

forming an electrically insulating layer on the floor of the trench; and

forming doped polysilicon on the electrically insulating layer, the doped polysilicon serving as the trench line.

25. The method of claim 24, wherein forming the first connector comprises diffusing dopants from the trench line through the first insert into a portion of the semiconductor substrate adjacent the first sidewall.

26. The method of claim 23, further including:

forming first and second gate structures adjacent the first sidewall of the first trench, the first and second gate structures each having first and second sides, wherein the first doped region is adjacent the second side of the first gate structure and the first side of the second gate structure and serves as a source region;

forming a first drain region adjacent the first sidewall of the first trench and adjacent the first side of the first gate structure; and

forming a second drain region adjacent the first sidewall of the first trench and adjacent the second side of the second gate structure.

27. The method of claim 26, further including forming a second trench in the semiconductor substrate, the second trench extending from the major surface into the semiconductor substrate and having first and second sidewalls and a floor.
28. The method of claim 27, further including:
forming a second trench line in the second trench; and
forming a third insert between the second trench line and the first sidewall of the second trench.
29. The method of claim 28, further including:
forming a fourth doped region adjacent the first sidewall of the second trench and spaced apart from the first drain region; and
forming a second connector between the fourth doped region and the first drain region.
30. The method of claim 29, further including:
forming a fifth doped region adjacent the first sidewall of the second trench and spaced apart from the second drain region; and
forming a third connector between the fifth doped region and the second drain region.
31. The method of claim 23, further including:
forming a bit line over the semiconductor substrate; and
electrically coupling the first drain region to the bit line.